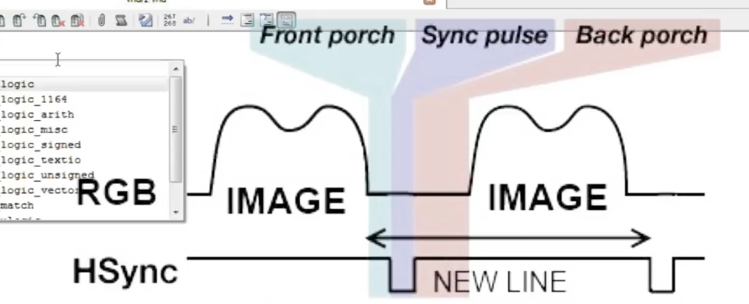
VGA interface consists of five signals: three 4-bit color channels(RGB), vertical sync and horizontal sync



Each line starts with LOW state on hsync signal.

Each frame with LOW state on vsync signal.

Before and after each sync pulse the RGB signals should also go LOW for a specific number of clk cycles

These are called front porch and back porch.

\*timing is very important, or else your monitor will not recognize the video signal\*

Pixelclock for 1280x1024 @ 60 hz is 108 Mhz I will use PLL to generate it from 24 Mhz onboard oscillator

VGA main entity WILL GET 24Mhz as main clk, VGA\_HS, VGA\_VS, VGA\_R, VGA\_G, VGA\_B.

Component sync will control all VGA signals and gets its own 108Mhz.

\*Horizontal line consists of 1280 visible pixels, 48 FP, 248 BP, and 112 sync pulse. sum:1688

\*Vertical line has 1024 visible pixels, 1 FP, 38 BP, and 3 for sync pulse. Sum:1066.

Current position is defined by HPOS and VPOS.

Each clk cycle, inc HPOS and once it hits EOL, reset to zero AND inc VPOS. (SCANNING LINE BY LINE)

Hsync goes LOW b/t FP and BP. If HPOS > 48(End of FP) AND HPOS < 160 (48FP + 112SYNC). ELSE HIGH

Same idea for Vsync b/t 0 and 4th line goes LOW else HIGH.

From beginning of FP til end of BP, RGB should be LOW.

T4, HPOS between 0 and 408 (FP+BP+SYNC) OR VPOS between 0 and 42, R/G/B = 0.

VGACLK is 108Mhz signal that will be generated.

First generate pixel clock from PLL using 24Mhz oscillator.

OPEN Qsys, Delete default component, Select PLL => Avalon ALTPLL, Reference input clk is 24MHz. Don’t need reset or locked signals, Ouput clk is 108Mhz, Extract important signals clkin, clkout and reset that will be used in the entity, Generate.

CLOSE Qsys, Open settings => add files => search for .qip files, and apply.

Copy and paste component portion into main file.

Pll will be instatiated with input as clock\_24, reset and output vgaclk AKA 108Mhz.